

A synchronous rectification method with a high-speed comparator for a megahertz frequency BWPT system to enhance efficiency

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Abstract

In bidirectional wireless power transfer (BWPT) systems, the phase synchronization accuracy of the secondary synchronous rectification (SR), or active rectification signal directly determines energy transfer efficiency and overall system stability. In traditional SR solutions, current transformers increase system losses. The auxiliary coil and RF line connection are susceptible to electromagnetic interference, resulting in signal delays, that lead to reduced system efficiency. This paper proposes a secondary-side self-synchronized rectification method that utilizes a high-speed comparator to perform real-time zero-crossing detection (ZCD) of the voltage across the secondary compensation capacitor, thereby generating a synchronization signal on the secondary side. By sampling the compensation capacitor, the obtained synchronization signal demonstrates high stability and strong immunity to interference. By studying synchronization signal acquisition at a switching frequency of 1 MHz, the proposed method enhances the stability of secondary-side synchronous rectification, enables soft switching, reduces system losses, and supports high-efficiency BWPT at 1 MHz. In this experiment, a BWPT system prototype incorporating a synchronous rectification method was developed. The system utilizes GaN devices in combination with an S-S compensation network and operates at a frequency of 1 MHz. SR is achieved on the secondary side, delivering an output power of 336.57 W, with a transmission efficiency of 96.48%.

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Introduction

With the rapid development of industrial fields^[1,2] such as consumer electronics, drones, robotics, electric vehicles, medical equipment, and bionic robotic dogs, smart mobile devices are being widely used in complex scenarios like disaster rescue, field exploration, and underwater wireless power transmission^[3–6]. In wireless power transfer (WPT) systems, the series-series (SS) compensation topology enables contactless energy transmission by eliminating the need for physical connectors. This feature significantly improves system reliability and durability by mitigating issues caused by corrosion, dust, and moisture in harsh environments^[7]. Additionally, the SS topology is structurally simple, allowing for the integration of the resonant capacitor and power converter onto a single PCB, which contributes to lightweight design and enhances power density—two critical factors in portable and space-constrained applications. Owing to these advantages, SS compensation networks have been widely adopted in various low- and mid-power WPT applications, including mobile robots, unmanned aerial vehicles (UAVs), smartphones, power banks, medical devices, and other consumer electronic products^[8–10]. Moreover, the simplicity of the SS configuration also facilitates ease of control and design scalability, making it a practical choice for both research prototypes and commercial implementations.

However, their ability to operate continuously faces significant challenges in power supply. As a result, bidirectional wireless power transfer (BWPT) has been rapidly advancing in these fields^[11,12]. In BWPT systems, compensation networks are typically chosen based on their suitability for bidirectional energy flow. Current-source-type compensation topologies are preferred, such as SS compensation, double-side LCC, and double-side LCL^[13–18]. To maintain stable power transfer, it is essential to keep the primary and secondary converters phase-synchronized. However, with the trend toward

higher frequencies and increased power density, especially in megahertz frequency-level systems driven by GaN devices, phase synchronization techniques face stringent requirements. Loss of synchronization signals can lead to increased power losses, reduced efficiency, loss of soft switching, zero voltage switching (ZVS), and even potential damage to power devices. These issues significantly affect the stability and practicality of BWPT systems.

In the application of BWPT, there is no direct-wired communication between the converters on both sides, making direct phase synchronization challenging^[19]. Traditionally, current transformers have been used to synchronize the phase signals of the converters to provide synchronization signals to the secondary-side converter^[20]. A method was employed to achieve synchronous rectification (SR) through a radio frequency (RF) wireless communication interface. However, due to the relatively high operating frequency of the converters and the inherent transmission delays in real-time communication, combined with the susceptibility of RF communication to electromagnetic interference, this method lacks sufficient stability. In a novel 16-ary pulse interval modulation simultaneous wireless power and data transfer scheme, based on a SS compensation topology, was proposed^[21]. Through this integrated power and data transmission method, the synchronization signal is transferred from the primary side to the secondary side, thereby enabling synchronous rectification. An inductive phase synchronization method, using an auxiliary winding, is proposed^[22]. This approach transmits synchronization signals based on the voltage across the auxiliary winding and the current through the magnetic coupling's secondary winding. However, it imposes strict electromagnetic compatibility requirements on the winding and is highly susceptible to interference, which can compromise system stability.

This paper presents a phase synchronization method for SR in BIPT systems that eliminates the need for communication links, sensors, or auxiliary windings, effectively addressing the demand

for high-speed synchronization. The method samples the voltage across the secondary compensation capacitor in the SS compensation network. After filtering and voltage division, the signal is fed into a high-speed comparator. The comparator generates a pulse signal, which is sent to the microcontroller unit (MCU). The MCU processes this signal, adjusts the phase and dead time, and controls the secondary-side switches to achieve SR. In contrast to traditional approaches, this method does not depend on current transformers, RF communication, or auxiliary coils, making it more resistant to electromagnetic interference. The proposed solution offers high stability, low cost, strong reliability, and high efficiency. Compared to integrated SR chips, the proposed scheme exhibits more stable and efficient operation under high-frequency conditions, while also enabling output power regulation.

Model of the BWPT system

System overview

A typical BWPT system is illustrated in Fig. 1. In this configuration, two bidirectional converters—one on the primary side and one on the secondary side—control the power flow. BWPT is achieved through coil coupling combined with its compensation network. It shows a common application of the full-bridge circuit within a BIPT system. In this circuit, switches Q_1 – Q_4 serve as the control switches for the primary-side full-bridge inverter, while switches Q_5 – Q_8 control the secondary-side full-bridge rectifier. L_p and L_s represent the self-inductance of the primary and secondary coupling coils, respectively, with M denoting their mutual inductance. U_{in} and U_{out} are input voltage and output voltage; U_1 and U_2 are the voltages generated by the full-bridge inverter on the primary side and the full-bridge rectifier on the secondary side, respectively; and I_1 and I_2 are the corresponding AC currents on the primary and secondary sides. The primary and secondary sides are designed with hardware to capture frequency and phase signals. Under MCU processing, phase shifting and dead time settings are applied to achieve SR during power transmission.

Analysis of the circuit based on SS compensation

The approach employed in this paper involves sampling at the zero crossing points of the compensation capacitors within the SS compensation network of the secondary side compensation. As illustrated in Fig. 2, this WPT topology features L_p and L_s , which denote the self-inductances of the primary and secondary magnetic coupling coils, respectively; R_p and R_s , which represent the internal resistances on the primary and secondary sides; C_p and C_s are

the compensation capacitors on both sides; R_L represents the DC constant load resistance in the BWPT system, while R_{eq} denotes the equivalent AC resistance. The following calculations detail the parameters of the S–S compensation network as^[22]:

$$\begin{cases} L_p C_p = \frac{1}{\omega^2} = \frac{1}{(2\pi f_s w)^2} \\ L_s C_s = \frac{1}{\omega^2} = \frac{1}{(2\pi f_s w)^2} \end{cases} \quad (1)$$

where, f_s and ω represent the switching frequency, and the angular switching frequency, respectively.

Thus, the primary-side reactance is denoted as X_p , and the secondary-side reactance as X_s :

$$\begin{cases} X_p = \omega L_p - \frac{1}{\omega C_p} \\ X_s = \omega L_s - \frac{1}{\omega C_s} \end{cases} \quad (2)$$

The equivalent impedances of the primary, secondary sides, and the equivalent resistance R_{eq} of the rectifier are^[22]:

$$\begin{cases} Z_p = R_p + jX_p \\ Z_s = R_s + jX_p \\ R_{eq} = 8\pi^{-2} R_L \end{cases} \quad (3)$$

In the resonant state, the currents of the primary and secondary sides can be obtained by combining Eqs (1) and (2) respectively:

$$\begin{cases} \dot{I}_1 = \frac{\dot{U}_1(R_{eq} + Z_s)}{Z_p(R_{eq} + Z_s) + (\omega M)^2} \\ \dot{I}_2 = \frac{j\omega M \dot{U}_1}{Z_p(R_{eq} + Z_s) + (\omega M)^2} \end{cases} \quad (4)$$

Based on Eq. (4) and R_{eq} , the system output voltage U_2 is:

$$\dot{U}_2 = \dot{I}_2 R_{eq} = \frac{j\omega M R_{eq} \dot{U}_1}{Z_p(R_{eq} + Z_s) + (\omega M)^2} \quad (5)$$

And based on the input voltage U_{in} and current I_1 , the input impedance Z_{in} and angle θ_{in} are:

$$\begin{cases} Z_{in} = \frac{\dot{U}_1}{\dot{I}_1} = \frac{Z_p(R_{eq} + Z_s) + (\omega M)^2}{(R_{eq} + Z_s)} \\ \theta_{in} = \tan^{-1} \left(\frac{\text{Im}[Z_{in}]}{\text{Re}[Z_{in}]} \right) \end{cases} \quad (6)$$

According to Kirchhoff's laws, the output impedance Z_{out} and its phase angle can θ_{out} be expressed as:

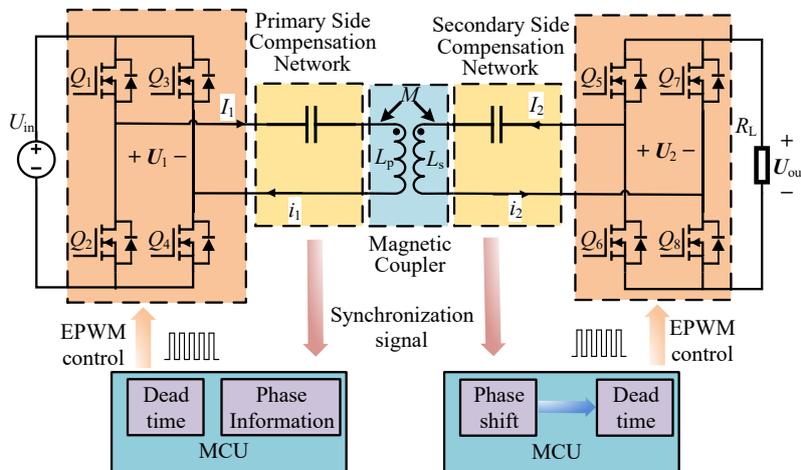


Fig. 1 A typical structure block diagram of the BWPT system.

$$\begin{cases} Z_{out} = Z_p + \frac{(\omega M)^2}{R_{eq}} \\ \theta_{out} = \tan^{-1} \left(\frac{\text{Im}[Z_{out}]}{\text{Re}[Z_{out}]} \right) \end{cases} \quad (7)$$

Based on Fig. 2 and Kirchhoff's laws, the ground-referenced voltages across the resonant capacitor on the secondary side can be derived as U_{cs1} and U_{cs2} , which are expressed as:

$$\begin{cases} \dot{U}_{cs1} = -j\omega M \dot{I}_1 \\ \dot{U}_{cs2} = -j\omega M \dot{I}_1 - \frac{1}{j\omega C_s} \dot{I}_2 \end{cases} \quad (8)$$

Thus, the voltage difference across the secondary-side resonant capacitors, denoted as U_{cs} , can be expressed as:

$$\dot{U}_{cs} = \dot{U}_{cs2} - \dot{U}_{cs1} = -\frac{M \dot{U}_1}{(Z_p(R_{eq} + Z_s) + (\omega M)^2) C_s} \quad (9)$$

Based on the input voltage U_{in} and the current expression in Eq. (4), the input power P_{in} and output power P_{out} can be derived as follows:

$$\begin{cases} P_{in} = \text{Re}(U_{in} \bar{I}_1) = \frac{U_{in}^2 (R_{eq} + R_s)}{R_p(R_{eq} + R_s) + (\omega M)^2} \\ P_{out} = \frac{(\omega M)^2 R_{eq} U_{in}^2}{(R_p(R_{eq} + R_s) + (\omega M)^2)^2} \end{cases} \quad (10)$$

And the system's output efficiency η can be expressed as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(\omega M)^2 R_{eq}}{(R_{eq} + R_s)[R_p(R_{eq} + R_s) + (\omega M)^2]} \quad (11)$$

For the SS compensation network, output power P_{out} can be regulated using phase-shift modulation (PSM). Based on Fig. 3, there exists a 90° phase difference between I_1 and I_2 when the circuit operates under resonant conditions^[23,24]. The switching waveforms of the inverter and the rectifier, along with I_1 , I_2 , U_1 , and U_2 , are illustrated in Fig. 3. When the PSM technique is applied to both the inverter and rectifier stages, the band-pass filtering property of the resonant compensation network allows for the use of the fundamental harmonic approximation to estimate the RMS values of U_1 and U_2 . Consequently, the following expression can be derived^[24]:

$$\begin{cases} U_1 = \frac{2\sqrt{\cos(\alpha) + 1}}{\pi} U_{in} \\ U_2 = \frac{2\sqrt{\cos(\beta) + 1}}{\pi} U_{out} \end{cases} \quad (12)$$

Therefore, power regulation can be realized by adjusting the output voltage U_{out} accordingly.

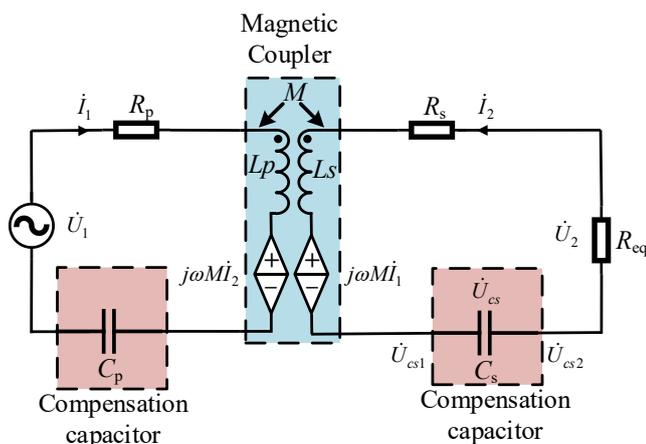


Fig. 2 Equivalent circuit of the BWPT system.

$$U_{out} = \frac{\pi}{2\sqrt{\cos(\beta) + 1}} U_2 \quad (13)$$

The proposed SR method with a high-speed comparator

Working mode

Since U_{cs1} and U_{cs2} have high voltages in the compensation network, and U_{cs2} is connected to the rectifier with a square wave voltage waveform, they cannot be directly fed into the comparator. Based on the characteristics of capacitors:

$$\begin{cases} di = C \frac{du}{dt} \\ Z_c = \frac{1}{j\omega C} \end{cases} \quad (14)$$

It is known that the voltage across a capacitor cannot change abruptly, making it suitable for stable voltage sampling. As shown in Fig. 4, this approach uses two capacitors, C_1 and C_2 , to filter out common-mode signals from U_{cs1} and U_{cs2} . Then, voltage divider resistors R_1 and R_2 are used to obtain the ground-referenced voltages U_1 and U_2 . These signals are then fed into a comparator, which generates a pulse signal for the MCU. Upon receiving the synchronization signal, the MCU applies phase shifting, and dead time control to the gate signals of Q_5 - Q_8 .

Due to the presence of the voltage divider resistors, the currents I_{c1} and I_{c2} are very small, only a few milliamps, and can be neglected

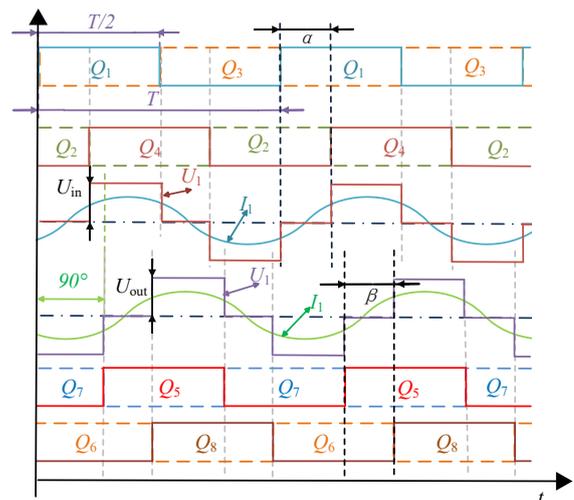


Fig. 3 Phase-shift modulation-based power control strategy for the S-S compensation topology.

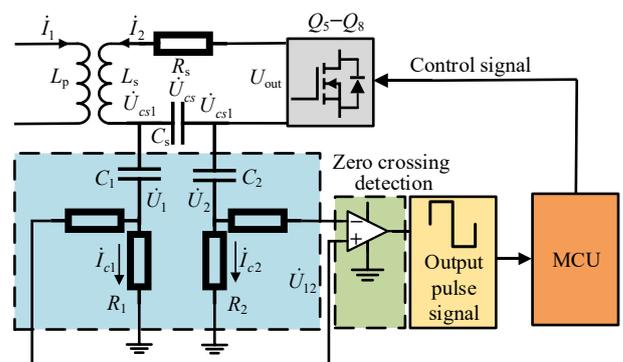


Fig. 4 Diagram of the circuit of the zero-crossing detection.

in I_2 . In Eqs (5) and (6), U_{cs1} and U_{cs2} have already been derived, and the ground-referenced branch resistance of U_{cs1} and U_{cs2} is given by:

$$\begin{cases} Z_1 = \frac{1}{j\omega C_1} + R_1 \\ Z_2 = \frac{1}{j\omega C_2} + R_2 \end{cases} \quad (15)$$

From Eq. (13), the sampled voltages U_1 and U_2 obtained by the high-speed comparator can be expressed as:

$$\begin{cases} \dot{U}_1 = \dot{U}_{cs1} \frac{j\omega C_1 R_1}{1 + j\omega C_1 R_1} \\ \dot{U}_2 = \dot{U}_{cs2} \frac{j\omega C_2 R_2}{1 + j\omega C_2 R_2} \end{cases} \quad (16)$$

Equations (5) and (6) show that U_{cs1} and U_{cs2} exhibit voltage and phase differences. Considering the same frequency and selecting $C_1 = C_2$ and $R_1 = R_2$. Solve Eqs (11) and (6) simultaneously to obtain:

$$\dot{U}_{12} = \dot{U}_1 - \dot{U}_2 = \frac{-j\omega C_1 M R_1 \dot{U}_1}{(1 + j\omega C_1 R_1)[(R_p(R_L + R_s) + (\omega M)^2)C_s]} \quad (17)$$

Based on the above equations, U_{cs} is processed through capacitive voltage division and common-mode signal filtering using C_1 and C_2 , resulting in voltage U_{12} . This voltage is then fed through a resistor into a high-speed comparator, which generates the synchronization signal V_{SYNC} for the MCU as shown in the timing diagram in Fig. 5. When $U_{12} > 0$, the high-speed comparator outputs a high-level signal, and when $U_{12} < 0$, it outputs a low-level signal. The high-speed comparator sends a pulse signal to the MCU upon obtaining the synchronization signal, as shown in Fig. 3. The MCU compares the pulse signal, adjusts the phase and pulse frequency, and controls the switching of Q_5 to Q_8 , achieving SR. Additionally, by controlling the dead time and phase, soft switching is realized on the secondary side, significantly reducing the turn-off losses of GaN devices and enhancing the overall system efficiency.

ZVS analysis of the system

A topology that enables ZVS is required to achieve a highly efficient and high-power-density converter. The realization of zero-voltage switching (ZVS) requires careful consideration of the parasitic capacitances inherent in power devices such as MOSFETs and GaN transistors. To ensure ZVS operation, the circuit must satisfy the following conditions^[25,26]:

$$\frac{1}{2} L I_1^2 \geq Q_{oss}(U_1) \cdot U_1 \quad (18)$$

There, $Q_{oss}(U_1)$ denotes the charge stored in the MOSFET's parasitic output capacitance C_{oss} when the drain voltage is U_1 . To mitigate the losses caused by hard switching in most MOSFETs,

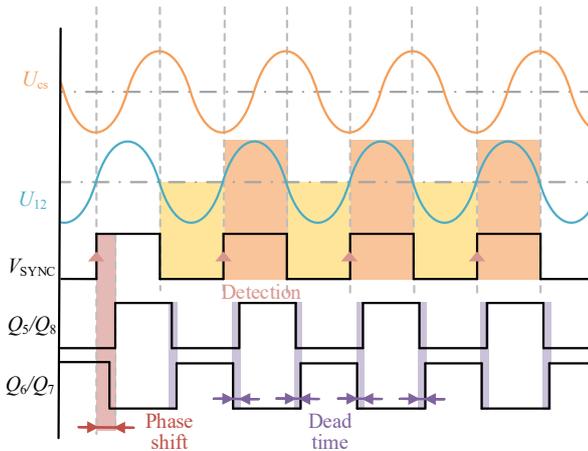


Fig. 5 Time sequence diagram of the proposed SR method signal.

ZVS is commonly employed to achieve soft switching. This requires an additional inductor current, which charges and discharges the parasitic capacitance of the relevant MOSFET.

For GaN and Si devices, switching losses are primarily concentrated in turn-off losses. Therefore, it is crucial to ensure that the charge $Q_{oss}(U_1)$ is fully discharged before switching transitions occur. Under these conditions, the voltage and current at the switching device should exhibit weak inductive characteristics. By sacrificing a small amount of non-resonant conduction loss, turn-off losses in the switching device can be significantly reduced.

For the inverter to achieve ZVS, the input impedance Z_{in} must exhibit inductive characteristics. In this experimental design, weak inductance is achieved by fine-tuning the resonant capacitor, thereby increasing the inductive component of Z_{in} at the original Zero Phase Angle (ZPA) point.

Due to the constant current source characteristics of the S-S compensation network, as described in Eqs (1) and (4), the resonant network and compensation capacitor remain unaffected by changes in the equivalent load R_{eq} . Instead, R_{eq} only alters the phase angle, as given in Eq. (6). Based on the turn-off current I_{OFF} of both the converter and the MOSFET, as well as the stability of the ZVS condition, the value of I_{OFF} for the reactance X_S can be derived from Eqs (4) and (6) as follows:

$$I_{OFF} = -\frac{2U_1 X_S}{\pi\omega^2 M^2} \quad (19)$$

From this equation, it can be deduced that there exists a maximum value of $|X_S|$, denoted as $X_{S,max}$, for the turn-off current I_{OFF} , which enables the MOSFET to achieve complete ZVS. The following equation can be derived:

$$X_{S,max} = -\omega^2 M^2 \pi \sqrt{\frac{Q_{oss}(U_1)}{2U_1 L_p}} \quad (20)$$

Thus, the resonant parameters can be calculated based on the value of $X_{S,max}$.

Since a full-bridge inverter is used in this experiment, U_1 is half of the input voltage of a half-bridge inverter. Therefore, the design value of $X_{S,max}$ in this experiment, is expressed as:

$$X_{S,max} = -\omega^2 M^2 \pi \sqrt{\frac{Q_{oss}(0.5U_1)}{2U_1 L_p}} \geq X_S \quad (21)$$

Phase angle constraint conditions for achieving ZVS in synchronous rectification and BWPT were proposed^[27,28]. Here, θ_{in} and θ_{out} represent the input impedance angles as defined in Eqs (6) and (9), respectively. Here, φ_p denotes the phase difference between the primary-side voltage θ_{U1} and current θ_{I1} , with D_p as the duty cycle of the primary switches. Likewise, φ_s represents the phase difference between the secondary-side voltage θ_{U2} and current θ_{I2} , while D_s is the duty cycle of the secondary switches.

$$\begin{cases} \varphi_p = \theta_{uin} - \theta_{i1} \\ \varphi_s = \theta_{uout} - \theta_{i2} \end{cases} \quad (22)$$

Neglecting parasitic parameters, φ_p can be approximated as θ_{in} , and φ_s as θ_{out} . According to the phase angle constraints for synchronous rectification presented in, the conditions for φ_p and φ_s are as follows^[29]:

$$\begin{cases} 0 \leq \varphi_p \leq \frac{\pi}{2} D_p \\ 0 \leq \varphi_s \leq \frac{\pi}{2} D_s \end{cases} \quad (23)$$

Using the values in Table 1, system parameters together with Eqs (1), (2), (19), and (20), the ZVS boundary conditions and network resonance are:

Although $X_{S,max}$ is very small, between 0 and 0.02 Ω , it is not zero; Fig. 6a shows how $X_{S,max}$ varies with frequency. Combining these

Table 1. System parameters.

Parameters	Symbol	Value
Input voltage	U_{in}	12–48 V
Primary inductance	L_p	1.79 μ H
Primary resonant capacitor	C_p	15.5 nF
Primary internal resistances	R_p	23 m Ω
Coil spacing	d	10 mm
Coupling coefficient	k	0.32
Load resistance	R_L	5 Ω
Secondary inductance	L_s	1.77 μ H
Secondary resonant capacitor	C_s	13.5 nF
Secondary internal resistances	R_s	28 m Ω
Switching frequency	f_{sw}	1 MHz
GaN's output capacitance	Q_{oss}	50 nC

Table 2. The ZVS boundary conditions and network resonance.

ZVS boundary conditions	Switching frequency (f_{sw}) (MHz)
$\phi_p = 0$	0.9034
$\phi_s = 0$	0.9582
$X_s = X_{s,max}$	1.0238
Network resonance: $X_s = 0$	1.0242

resonance to satisfy the ZVS criteria introduces a small amount of additional conduction loss but substantially reduces switching loss, leading to a significant improvement in overall system efficiency.

Experimental verification

Experimental prototype

This experiment employs a hollow coil along with an integrated design of the compensation capacitor and converter. This integrated design benefits from allowing for precise signal acquisition while minimizing electromagnetic interference from the coil. In light of these considerations and the proposed method, an experimental platform was established, as shown in Fig. 7.

constraints yields the ZVS operating range in Fig. 6b, where ZVS is achieved when:

$$0.9582 \text{ MHz} < f_{ZVS} < 1.0238 \text{ MHz} \quad (24)$$

Under the design conditions of Table 2, choosing $f_{sw} = f_{ZVS}$ places the system firmly within this ZVS region. Operating slightly off

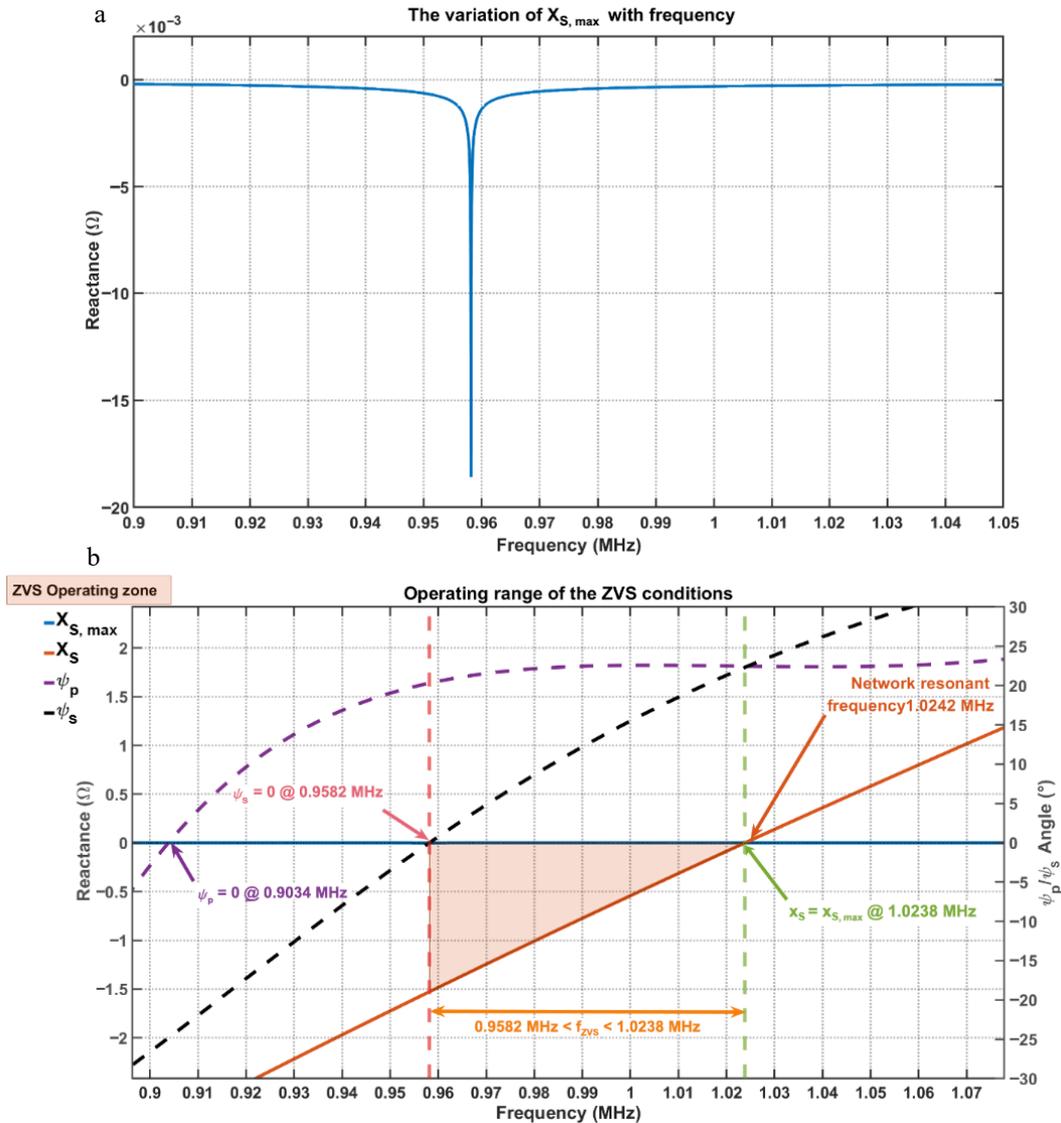


Fig. 6 Operating range of the ZVS conditions. (a) The variation of $X_{s,max}$ with frequency. (b) The range of ZVS.

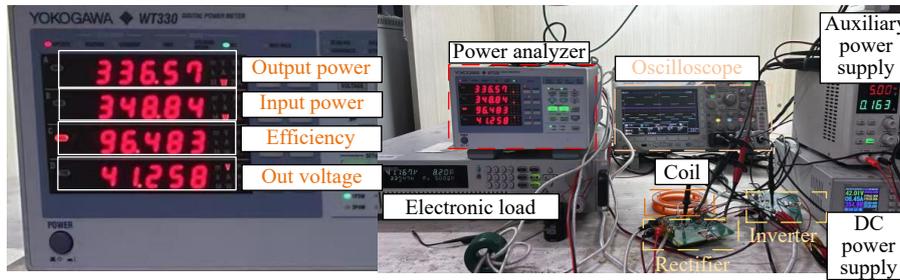


Fig. 7 Experimental platform and max efficiency.

In this experiment, the system operates at a switching frequency of 1 MHz, and the coupling coil has a diameter of 1 mm. The coils feature an air-core design and are constructed using multi-strand Litz wire along with 3D-printed components. The type of resonant capacitors is the NP0 capacitors. Both the primary and secondary converters are implemented on identical PCB boards with the same components, employing full-bridge converter topologies. The switching devices are GaN (ISG32001) components, with power diodes (NSR20F40NXT5G) paralleled with GaN devices to protect the system. The main control boards are built on the FPC (Flexible Printed Circuit) module. The control chip used on both sides is the C2000 MCU (TMS320 F2800137), and the high-speed comparator employed is GS8743. A 42V DC power supply provides the transmission power, while a 5.5 V auxiliary power supply powers the main control MCU, gate drive circuits, and comparators. The load is a 5 Ω constant-resistance electronic load, and a power analyzer is used to measure transmission efficiency. The specific experimental parameters are listed in Table 1, where U_{out} represents the output voltage, d represents the distance between the two coils, and k is the coupling coefficient of the coupled coil. According to the datasheet of the GaN device (ISG32001), the value of Q_{oss} is obtained. Here, t_d represents the dead time, and D is the duty cycle of the switching square wave.

In WPT systems, the secondary side often employs passive rectification. This approach stems from the difficulty in synchronizing the oscillators and MCU clock frequencies between the primary and secondary sides, leading to challenges in aligning gate drive signal periods without auxiliary synchronization mechanisms. Traditional BIPT systems typically require communication lines, current transformers, or auxiliary coils to synchronize the MCU or gate signals on both sides. This paper proposes a method utilizing a high-speed comparator to perform the ZCD on the voltage across the secondary compensation capacitor. By implementing this technique, signal synchronization between the secondary and primary sides is achieved. The following section presents experimental verification of the ZCD method under the design parameters listed in Table 1, System parameters, demonstrating SR at a 1 MHz switching frequency.

Experimental results

Based on the mentioned theories and analyses, an experimental platform was established to validate the proposed method. The experimental waveform of the secondary-side synchronous signal is shown in Fig. 8a. At the switching frequency of 1 MHz, the voltage waveform across the compensation capacitor C_s , denoted as U_{cs} , is observed. Due to the high amplitude of U_{cs} it cannot be directly connected to the high-speed comparator. Therefore, after passing through a common mode circuit, it eliminates harmonic signals, it avoids the influence of the rectifier switch tube, and makes the U_{cs} a sinusoidal voltage. Then, in its divider circuit, ZCD is performed using the comparator, resulting in the synchronous signal U_{cs} . This signal is then utilized by the MCU to synchronize the clock and gate drive signals on the secondary side, producing synchronized gate

signals for Q_5/Q_8 , as illustrated in Fig. 8c. In Fig. 8a, the ZCD signal U_s and the Q_5/Q_8 pulse emitted by the secondary-side MCU achieve stable synchronization. By dead time and phase settings in the MCU,

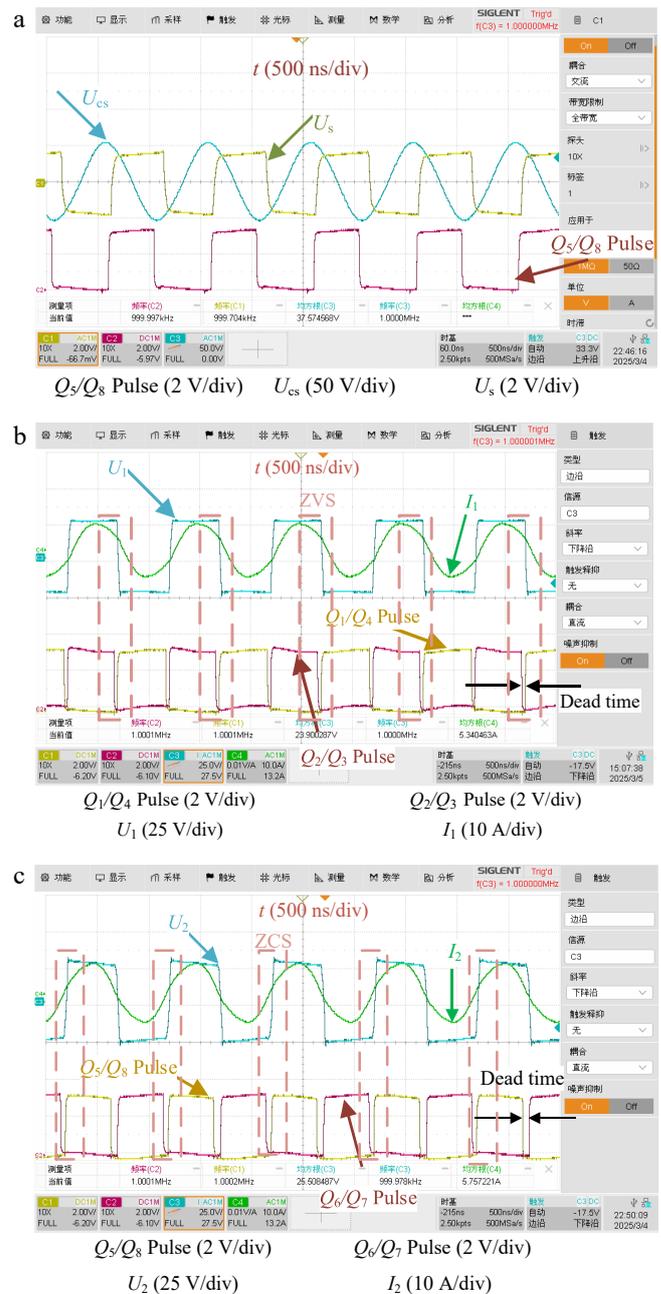


Fig. 8 Soft-switching and synchronous signal. (a) Secondary synchronous signal sampling experimental waveform. (b) Primary waveform. (c) Secondary waveform.

synchronization is also maintained for Q_6/Q_7 , as shown in Fig. 8c. Ultimately, this method achieves signal synchronization between the secondary and primary sides without the use of current transformers, communication methods, or auxiliary coils.

Under operating conditions of a constant input voltage $U_{in} = 24$ V, a constant-voltage electronic load output $U_{out} = 24$ V, and a system switching frequency of 1 MHz, ZVS is achieved through the MCU's dead-time control of the GaN drive signals and the compensation capacitors. Fig. 8b illustrates the primary side's waveform of ZVS and GaN's gate control signals. By maintaining the switching frequency of 1 MHz on the primary side and appropriately configuring the resonant network and dead time settings, ZVS is realized on the primary side. In Fig. 8b, U_1 represents the inverter voltage, I_1 denotes the current, and Q_1/Q_4 and Q_2/Q_3 correspond to the gate signals of the primary-side GaN switches.

Under operating conditions with a constant input voltage $U_{in} = 24$ V, a constant resistance electronic load $R_L = 5 \Omega$, and a system switching frequency of 1 MHz, ZVS was achieved through the MCU's dead-time control of the GaN drive signals and the use of compensation capacitors. As shown in Fig. 8b, the primary waveform illustrates the primary side's soft-switching waveform and the gate control signals of the GaN devices. By maintaining a 1 MHz switching frequency on the primary side and appropriately configuring the resonant network and dead-time settings, ZVS was successfully implemented. In Fig. 8b, U_1 represents the inverter's output voltage, i_1 denotes the inverter's output current, and Q_1/Q_4 and Q_2/Q_3 correspond to the gate signals of the primary side GaN switches.

Based on the theory presented in the SR method and as illustrated in Fig. 8a, stable synchronization signals were obtained during experiments. After implementing phase shifting and dead-time adjustments, the secondary MCU effectively synchronizes the operation of switches Q_5, Q_6, Q_7 , and Q_8 with the primary switches Q_1, Q_2, Q_3 , and Q_4 . This synchronization eliminates potential frequency discrepancies and unstable phase differences between the primary and secondary switches, thereby preventing erroneous conduction that could lead to secondary-side short circuits.

Similarly, in Fig. 8c, U_2 represents the voltage entering the rectifier from the compensation capacitor, i_2 denotes the corresponding current, and Q_5/Q_8 and Q_6/Q_7 are the gate signals for the secondary GaN devices. Through the combined effects of the compensation network and appropriate dead-time settings, soft-switching was

achieved on the secondary side. The low on-resistance of active devices reduced the voltage drop losses associated with passive rectifier power diodes, thereby enhancing system efficiency at a 1 MHz switching frequency. Under these operating conditions, the system achieved a maximum efficiency of $\eta_{max} = 96.48\%$ and an output power of 336.57 W, as depicted in Fig. 7.

Under the constant resistance mode of the electronic load with $R_L = 5 \Omega$, the system was tested at input voltages U_{in} of 12, 18, 24, 30, 36, 42, and 48 V. As shown in Fig. 9, both output power P_{out} and efficiency η vary with the input voltage. Across all tested conditions, the overall system efficiency remained above 96%. The max efficiency η of 96.48% was achieved at an input voltage of 42 V, corresponding to P_{out} of 336.57 W. Throughout the tested voltage range of 12–48 V, the primary side consistently operated under ZVS, while the secondary side maintained soft switching and low-loss performance through synchronous rectification. This rectification scheme ensured high efficiency and strong system stability.

A comprehensive loss analysis of the system is presented here. It should be noted that the GaN gate drivers and the MCU are powered by an auxiliary power supply; therefore, the losses associated with the auxiliary power supply are not included in the following analysis. As illustrated in Fig. 7, the total measured power loss in the system is 12.580 W. The power losses are categorized into four main components: inductor losses, capacitor losses, converter losses^[30,31], and other losses^[31,32]. The 'other losses' primarily include the effects of parasitic parameters on the PCB, losses in the power analyzer connection cables, and energy dissipation in the output bus capacitors across U_{out} . Based on a detailed analysis of the inductor, capacitor, and GaN device losses, the power distribution is summarized in Fig. 10. From this figure, it can be observed that inductor losses constitute the largest proportion of the total losses, followed by capacitor losses. The power loss contributed by GaN devices in the converter is only 2.533 W, accounting for 20.1% of the total. These results indicate that the proposed scheme demonstrates excellent efficiency on the converter side, achieving very low switching and conduction losses in the synchronous rectification stage.

Comparison with other works

Compared to other SR methods listed in Table 3, the system proposed in this work demonstrates superior robustness in terms of efficiency. When compared with the same SS compensation

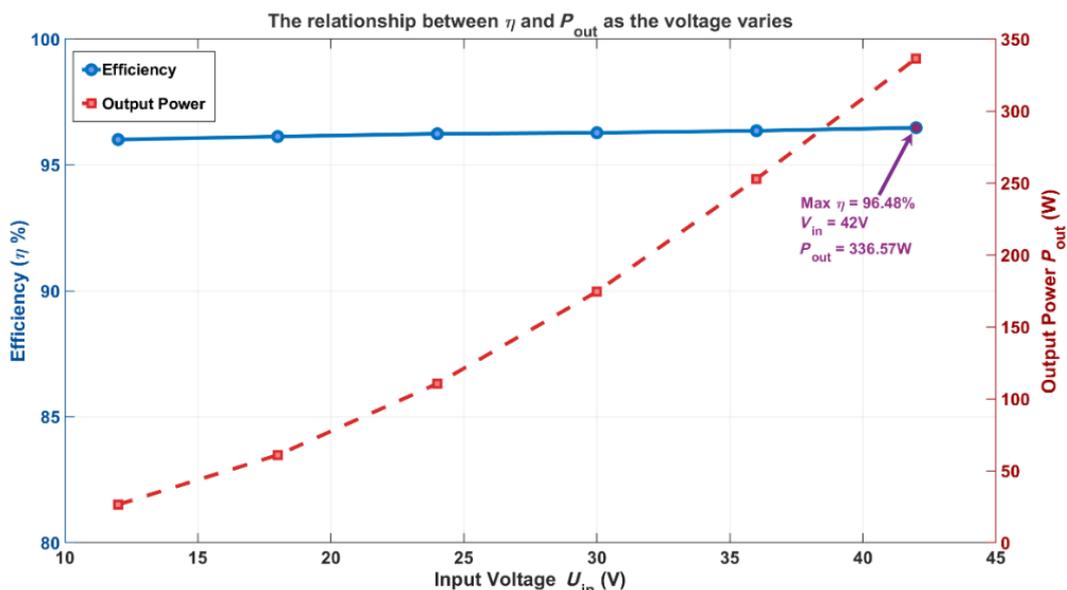


Fig. 9 Relationship between η and P_{out} when the R_{eq} is 5 Ω .

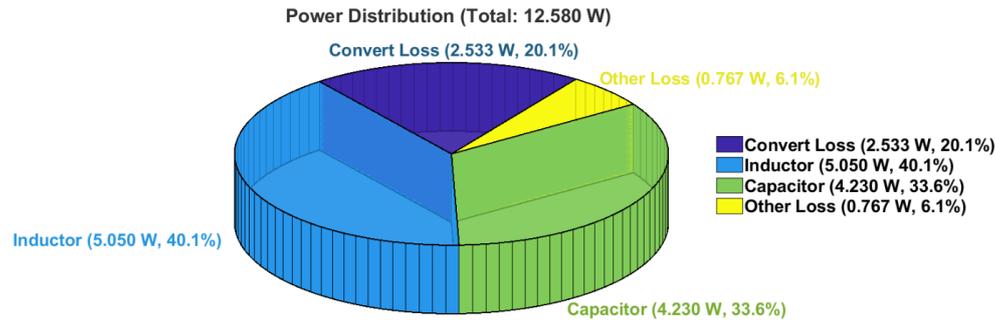


Fig. 10 Power loss distribution.

Table 3. Comparison with other works.

Frequency (Hz)	Coupling coefficient	Output power (W)	η_{\max}	Ref.
360 k	0.75	56	92.5%	[27]
150 k	–	46.19	86.4%	[33]
100 k	0.31	1,000	95.5%	[30]
800 k	–	35	95.0%	[34]
6.78 M	–	15	92.3%	[35]
6.78 M	0.2	17	82%	[36]
120 k	0.8	50	83%	[37]
1 M	0.32	336.57	96.48%	This work

network^[34], the proposed method achieves higher efficiency even at a higher switching frequency. Additionally, in comparison with the Class-E converters^[27], the proposed system still maintains a higher efficiency. Unlike Class-E converters, the full-bridge converter used in this experiment includes more switching devices. Despite the increased number of switches, the system still achieves efficient and highly stable power transfer. Across various SR strategies and compensation networks, this solution consistently delivers high efficiency and stability. Moreover, the hardware implementation of the ZCD is cost-effective, offers reliable signal performance, and is less susceptible to electromagnetic interference. In comparison with highly integrated commercial SR chips, the proposed SR scheme exhibits superior performance under high-frequency operating conditions, with significantly reduced power loss. Moreover, it enables output power regulation through MCU-based control, offering greater flexibility and adaptability in system-level design and application. This makes the proposed approach not only more efficient but also more extensible and scalable for practical engineering implementations.

Conclusions

This paper proposed a synchronous rectification method with a high-speed comparator for a Megahertz frequency BWPT system. Although the experimental analysis in this study focuses solely on the SS topology, the proposed synchronous rectification scheme is also applicable to other compensation topologies, such as dual-sided LCC, LLC-S, and dual-sided LLC. In these configurations, the scheme can similarly obtain complete synchronization signals, and achieve stable zero-crossing detection. Compared to integrated synchronous rectification (SR) chips, the proposed scheme offers superior frequency performance and significantly lower power losses. Furthermore, it provides a flexible platform for functional expansion and system-level customization. Unlike traditional approaches that rely on current transformers or auxiliary coils, this method directly connects the voltage across the secondary compensation capacitor to a comparator to acquire the synchronization signal. This signal is then processed by the MCU to achieve efficient SR on the secondary side. This method not only ensures

high-precision synchronization between the primary and secondary sides but also simplifies system design and enhances overall integration. Therefore, this method reduces losses on the secondary side and enhances overall system efficiency, demonstrating high stability at a switching frequency of 1 MHz while delivering an output power of 336.57 W with a transmission efficiency of 96.48%. Additionally, the approach is minimally affected by electromagnetic interference, features a simple hardware implementation, and offers low cost, making it highly versatile and widely applicable.

Author contributions

The authors confirm contributions to the paper as follows: study conception and design: Liu Z, Sun Z, Rong E; data collection: Yang Y, Zou X, Shafiq Z; analysis and interpretation of results: Li S, Li T, Yang Y, Lu S; draft manuscript preparation: Yang Y, Liu Z; conceptualization, funding acquisition, and supervision: Li S, Liu Z. All authors reviewed the results and approved the final version of the manuscript.

Data availability

The datasets generated and/or analyzed during the current study are available from the corresponding author upon reasonable request.

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Conflict of interest

The authors declare that they have no conflict of interest.

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