Wireless Power Transfer

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https://doi.org/10.48130/wpt-0026-0009

Wireless Power Transfer **2026**, 13: e020

Research on diagnosis of open-circuit fault in power switch of WPT system based on DC bus voltage and switch driving signal

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Abstract

Wireless power transfer (WPT) technology finds extensive applications in areas such as powering deep-sea exploration equipment. However, due to harsh operating environments, core components such as power switches are prone to failure, leading to system malfunctions. To address system abnormalities caused by open-circuit faults in WPT system power switches, this paper proposes a fault diagnosis method based on DC bus voltage and switch drive signals. First, the primary current paths during normal operation in zero-voltage switching mode are analyzed. The impact of a single power switch failure on system transmission characteristics is investigated, revealing that the fault reduces output power to approximately one-quarter while efficiency shows a slight decline. Second, a DC bus voltage model for the WPT system is established based on the current paths. By leveraging the disappearance of post-fault voltage characteristics in conjunction with switch drive signals, precise fault diagnosis and localization can be achieved. Finally, an experimental platform was constructed under different coupling conditions and load scenarios. Through simulating an open-circuit fault of the power switch, the impact of the fault on system transmission performance and the effectiveness of the proposed diagnostic method are verified.

Keywords: Wireless power transfer, Power switch, Open-circuit fault, Fault diagnosis, Fault location

Citation: Chen C, Wang F, Wang Z, Yu Y, Deng Q. 2026. Research on diagnosis of open-circuit fault in power switch of WPT system based on DC bus voltage and switch driving signal. *Wireless Power Transfer* 13: e020 https://doi.org/10.48130/wpt-0026-0009

Introduction

Wireless power transfer (WPT) technology, with its unique advantage of contactless energy delivery, has been widely adopted in fields such as electric vehicle charging and power supply for deep-sea exploration equipment[1,2]. A typical WPT system employs numerous power electronic devices, which may fail under harsh operational conditions, leading to system malfunction. Thus, research on fault diagnosis for WPT systems holds significant theoretical and practical importance. Current academic efforts in this area can be broadly classified into three categories: fault-tolerant control, machine learning, and signal processing.

Fault-tolerant control methods enhance system reliability through topology and control optimization. For instance, a dual-coupled LCC-S topology was introduced to achieve fault tolerance by utilizing the mutual inductance characteristics of coils[3], whereas another approach localized short-circuit faults via series sampling resistors at a relatively high cost[4]. Multi-transmitter/receiver architectures can enhance fault tolerance through redundant design[5,6]. Additionally, systems with incipient faults have been parameterized and stabilized using observer-based controllers[7−9]. However, these strategies primarily serve as emergency responses after a fault occurs, mitigating its impact without locating or eliminating the root cause.

Machine learning methods often abstract key units such as inverters, resonators, and rectifiers into independent subsystems. By collecting electrical parameters before and after a fault to build training datasets, artificial intelligence algorithms like backpropagation neural networks and support vector machines are applied to extract fault features, enabling defect identification in S-S and LCC-S type WPT systems[10]. Although this approach avoids complex physical modeling, it faces notable limitations: fault feature extraction is tightly coupled to specific system topologies, algorithm performance is highly sensitive to sample size, and heavy reliance on large labeled datasets restricts cross-topology transferability and real-time diagnostic efficiency.

To address the dependence of machine learning on massive training data, one study collected gate signals and switch currents under various operating conditions, employed rough set theory for feature extraction and redundancy removal, converted the results into logical expressions, and implemented fault diagnosis using digital logic modules[11], albeit with considerable diagnostic complexity. Another work designed a novel rectifier topology that maintains efficient operation under diode open-circuit conditions and diagnosed faults based on the appearance of a DC bias under failure, which is absent during normal operation[12]. Nevertheless, this solution has not been verified for switching device faults.

Power switch faults are generally categorized into short-circuit (SC) and open-circuit (OC) types. SC faults can normally be cleared by fast-acting fuses, whereas OC faults do not cause immediate system breakdown but increase electrical stress on healthy components, potentially leading to abnormal operation or damage over time. Based on the above analysis, this paper proposes a signal-processing method utilizing DC bus voltage and switch driving signal for diagnosis and localization of power switch OC fault in the WPT system. The remainder of the paper is organized as follows: firstly, analyzing the system transmission characteristics under the single-tube OC fault condition; secondly, designing the signal processing method based on the current path, and realizing the diagnosis and localization of the OC fault by identifying the disappearance of the specific voltage characteristics under the fault condition; and lastly, verifying the validity of the method through experiments.

https://doi.org/10.48130/wpt-0026-0009

Analysis of the system operating modal, current path, and transmission characterization

Topology of the proposed circuit

Figure 1 shows a typical S-S type WPT system used for fault diagnosis analysis in this paper. In this system, U_o is a DC voltage source, and the inductance L_1 and capacitance C_5 form a DC-side LC filter circuit. The stray inductance L_s is composed of the equivalent series inductance of C_5 and the line inductance. S_1 to S_4 are IGBT modules, with their respective anti-parallel diodes being D_1 to D_4 and parasitic capacitances being C_1 to C_4. These components collectively form a single-phase full-bridge inverter circuit. R_T, L_T, and C_T are the equivalent series resistance, resonant inductance, and resonant capacitance of the transmitter-side circuit, respectively. R_R, L_R, and C_R are the equivalent series resistance, resonant inductance, and resonant capacitance of the receiver-side circuit, respectively. M is the mutual inductance. Diodes D_5 to D_8, together with filter capacitor C_6, form a single-phase uncontrolled rectifier circuit. R_L is the load, and $R_E = \pi^2/8R_L$ is the equivalent resistance of the rectifier circuit[13]. The equivalent input impedance Z_{in} of the system can be expressed as:

$$Z_{in} = R_T + j(\omega L_T - 1/\omega C_T) + \frac{(\omega M)^2}{R_R + R_E + j(\omega L_R - 1/\omega C_R)} \tag{1}$$

where, ω is the operating angular frequency of the system.

Analysis of the main current paths in system ZVS operating mode

In the WPT system, to reduce switching losses, a phase-shift control strategy is typically used to operate the system in zero-voltage switching (ZVS) mode. Figure 2a shows the steady-state operating waveform of the system's inverter circuit output. Define U_{dc} as the input voltage of the inverter circuit. Under ideal conditions, ignoring the dead time t_d and various losses, the output voltage of the inverter circuit can be characterized by the phase shift angle δ:

$$U_{in} = \frac{2\sqrt{2}U_{dc}\cos(\delta/2)}{\pi} \tag{2}$$

When the system is operating normally, its current flow path corresponds to ten operating modes. To simplify the analysis process, this paper only focuses on the operating mode of the positive half-cycle of the current, as shown in Fig. 2b.

Mode 1, corresponding to the t_0–t_1 time interval: Apply drive signals to S_1 and S_4, and the current flows along the path $S_1 \rightarrow$ transmitter side circuit $\rightarrow S_4$.

Mode 2, corresponding to the t_1–t_2 time interval: Apply a drive signal to S_4, and S_1 is turned off in ZVS mode. At this point, the current flows through two paths: one path flows through $C_1 \rightarrow$ transmitter side circuit $\rightarrow S_4$ to charge C_1, and the other path flows through $C_2 \rightarrow$ transmitter side circuit $\rightarrow S_4$ to discharge C_2, preparing for the ZVS conduction of S_2. To ensure the ZVS margin, assuming that $C_1 = C_2 = C_3 = C_4 = C_{oes}$, we have[14]:

$$t_{12} = \frac{2C_{oes}U_{dc}}{I_{Tm}} \leq \frac{t_d}{2} \tag{3}$$

where, t_{12} is the duration of this mode.

Mode 3, corresponding to the t_2–t_3 time interval: Apply drive signals to S_2 and S_4. Since the IGBT module cannot conduct in reverse, the current flows through the path $D_2 \rightarrow$ transmitter side circuit $\rightarrow S_4$.

Mode 4, corresponding to the t_3–t_4 time interval: Apply a drive signal to S_2. Since the IGBT module cannot conduct in reverse, the current flows through two paths at this time: one path flows through $D_2 \rightarrow$ transmitter side circuit $\rightarrow C_4$ to charge C_4, and the other path flows through $D_2 \rightarrow$ transmitter side circuit $\rightarrow C_3$ to discharge C_3, preparing for S_3 ZVS conduction. To achieve system ZVS, it is necessary to ensure that Z_{in} exhibits resistive-inductive characteristics. Additionally, in engineering applications, a margin of 10~15° is typically reserved to meet the following relationship:

$$\arctan(Z_{in}) = (10 \sim 15)^\circ + \frac{\delta + \omega t_d}{2} \tag{4}$$

Mode 5, corresponding to the t_4–t_5 time interval: Apply drive signals to S_2 and S_3. Since the IGBT module cannot conduct in reverse, the current flows through the path $D_2 \rightarrow$ transmitter side circuit $\rightarrow D_3$.

System transmission characteristics analysis

(1) Normal working conditions

The transmission efficiency of the WPT system can be defined by the system output power P_{out} and the total system power loss P_{loss}:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{(2I_{Rm}/\pi)^2 R_L}{(2I_{Rm}/\pi)^2 R_L + P_{loss}} \tag{5}$$

where, I_{Rm} is the maximum value of the system receiver-side loop current i_R. The following section presents calculations for P_{loss}, which consist of four parts: LC filter circuit loss, inverter circuit loss, resonance compensation circuit loss, and rectifier circuit loss.

LC filter circuit loss: This loss is the thermal loss generated by the equivalent series resistance r_{L1} of the L_1 branch and the equivalent series resistance r_{C5} of the C_5 branch, denoted as P_{L1} and P_{C5}, respectively. Assuming that U_{dc} remains constant, the above two losses can be expressed as:

$$P_{L1} = I_o^2 r_{L1} \approx \left(\frac{I_{Tm}}{\sqrt{2}}\right)^2 r_{L1} \tag{6}$$

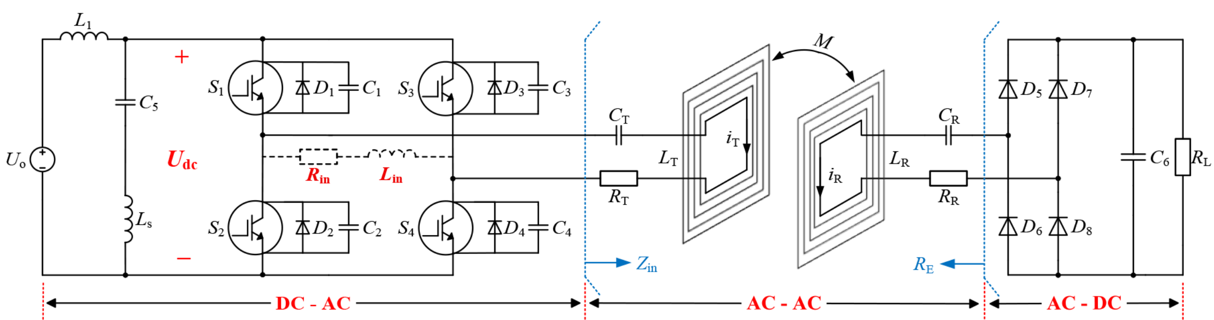

Fig. 1 A typical S-S type WPT system circuit topology diagram used for analysis in this paper.

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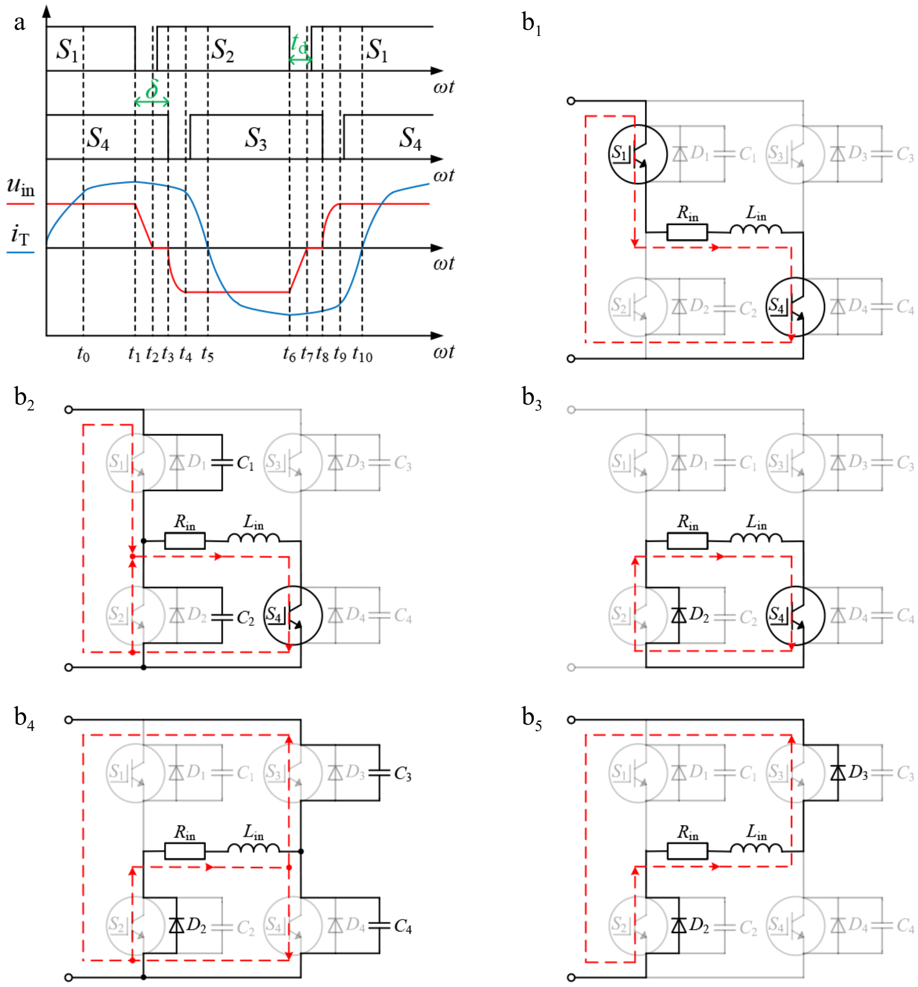

Fig. 2 Main current paths in the inverter circuit. (a) Inverter steady-state output waveform diagram. (b) Current paths in different operating modes within half a cycle. (b_1) Mode 1, corresponding to t_0–t_1. (b_2) Mode 2, corresponding to t_1–t_2. (b_3) Mode 3, corresponding to t_2–t_3. (b_4) Mode 4, corresponding to t_3–t_4. (b_5) Mode 5, corresponding to t_4–t_5.

$$P_{C5} = \left(\frac{I_{Tm}}{\sqrt{2}} - I_o\right)^2 r_{C5} \tag{7}$$

where, I_o is the current output from the voltage source, and I_{Tm} is the maximum value of the transmitter-side loop current i_T of the system.

Inverter circuit loss: This loss consists of three parts: the conduction loss P_{rs}, turn-on loss P_{ton}, and turn-off loss P_{toff} of the IGBT module. Among these, P_{rs} is the thermal loss generated by the conduction resistance r_{IGBT} of the switching transistor, P_{ton} is the thermal loss generated during the charging and discharging process of the capacitance C_{ce} between the collector and emitter of the IGBT, and P_{toff} is the power loss generated by the overlap of voltage and current during the turn-off process of the IGBT. The three components satisfy the following relationships[15]:

$$P_{rs} = \left(\frac{I_{Tm}}{\sqrt{2}}\right)^2 r_{IGBT} \tag{8}$$

$$P_{ton} = 10 f C_{ce} \sqrt{U_{dc}^3} \tag{9}$$

$$P_{toff} = f U_{dc} \frac{I_{Tm}}{\sqrt{2}} \left(\frac{t_r}{3} + \frac{t_f}{2}\right) \tag{10}$$

where, f is the operating frequency of the system, t_r is the voltage rise time of the switching transistor, and t_f is the current fall time.

Resonance compensation circuit loss: This loss, P_{comp}, consists of thermal losses generated by the equivalent series resistance of the transmit and receive side loops:

$$P_{comp} = \left(\frac{I_{Tm}}{\sqrt{2}}\right)^2 R_T + \left(\frac{I_{Rm}}{\sqrt{2}}\right)^2 R_R \tag{11}$$

Rectifier circuit loss: This loss consists of two parts: diode power loss P_D and C_6 branch loss P_{C6}. P_D is caused by the power loss resulting from the forward voltage drop U_D of the diode and the thermal loss generated by the forward resistance r_D. P_{C6} is the thermal loss generated by the equivalent series resistance r_{C6} of the branch where C_6 is located. The two meet the following relationships:

$$P_D = U_D \frac{I_{Rm}}{\pi} + \left(\frac{I_{Rm}}{2}\right)^2 r_D \tag{12}$$

$$P_{C6} = \left(\frac{2}{\pi} I_{Rm}\right)^2 \left(\frac{\pi^2}{8} - 1\right) r_{C6} \tag{13}$$

Substituting Eqs. (6)–(13) into Eq. (5) yields the following expression for the system transmission efficiency:

$$\eta = \frac{P_{out}}{P_{L1} + P_{C5} + 2P_{rs} + 4P_{ton} + 4P_{toff} + P_{comp} + 4P_D + P_{C6} + P_{out}} \tag{14}$$

(2) Inverter circuit single tube OC fault condition

Assuming an OC fault occurs in S_2, the primary current flow path in the system changes from the normal state of $D_1D_4 \rightarrow S_1S_4 \rightarrow D_2S_4 \rightarrow D_2D_3 \rightarrow S_2S_3 \rightarrow D_1S_3$ to $D_1D_4 \rightarrow S_1S_4 \rightarrow D_2S_4 \rightarrow D_2D_3 \rightarrow D_1S_3$, as shown in Fig. 3. During the negative half-cycle, the conductive path formed by D_2D_3 causes the inverter circuit to produce a reverse output voltage with a duration of t_{45}, as shown in Fig. 3b. This mode

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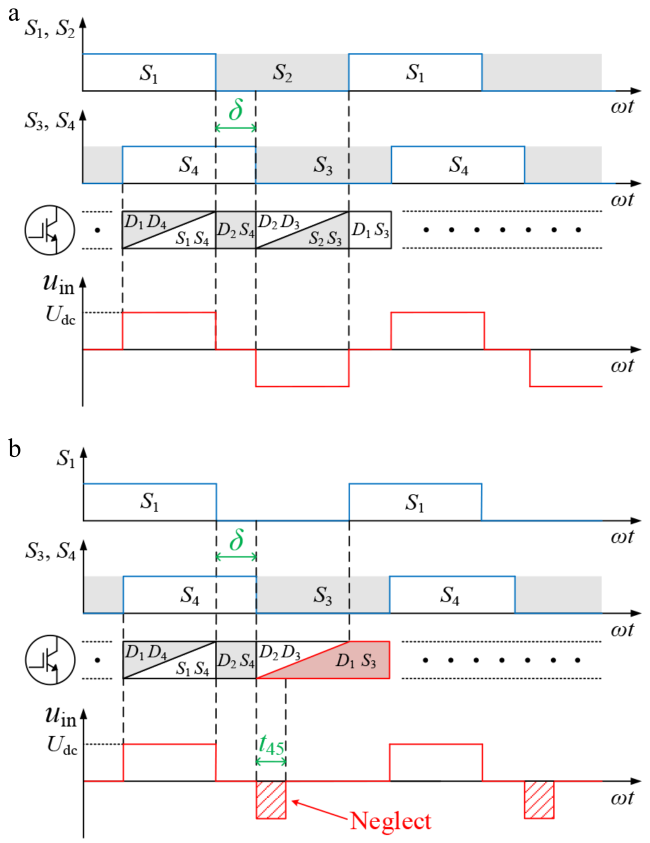

Fig. 3 PWM waveforms of switching devices under different operating conditions. (a) Normal working conditions. (b) S_2 OC fault condition.

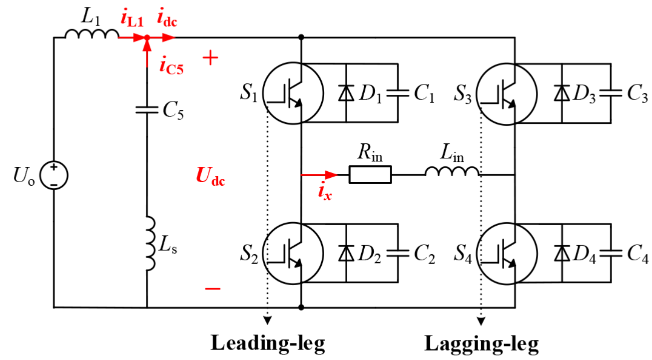

Fig. 4 Equivalent circuit topology of the WPT system used to establish the diagnostic model.

persists until the output current crosses zero in the reverse direction. t_{45} can be approximately by the switching tube leakage current I_{off}:

$$t_{45} = \frac{I_{off}\mathrm{Im}(Z_{in})}{U_{in} - I_{off}\mathrm{Re}(Z_{in})} \approx \frac{I_{off}L_{in}}{U_{in}} \tag{15}$$

Since the typical value of I_{off} is 10 to 100 μA, t_{45} can be neglected relative to the entire switching cycle under high voltage conditions. At this point, the output voltage of the inverter circuit after a single tube OC fault becomes:

$$U'_{in} = \frac{\sqrt{2}U_{dc}\cos(\delta/2)}{\pi} \tag{16}$$

From Eqs. (2) and (16), it can be deduced that after a fault occurs, the RMS value of the inverter circuit output voltage drops to half of the normal operating condition, causing I_{Tm} and I_{Rm} to drop to half of their original values. Considering that only three switching transistors are involved in the operation of the inverter circuit during the fault state, Eq. (14) becomes:

$$\eta' = \frac{P_{out}}{P_{L1} + P_{C5} + (I_{Tm}/\sqrt{2})^2 r_{C5} + 3P_{rs}/2 + 12P_{ton} + 6P_{toff} + P_{comp} + 4P_D + 4U_D I_{Rm}/\pi + P_{C6} + P_{out}} \tag{17}$$

In Eq. (17), P_{out} dominates. Comparing with Eq. (14), it can be seen that the system efficiency decreases slightly after the fault, while the output power drops significantly to about one-quarter of the normal operating condition. In actual experiments, the specific numerical value of the efficiency reduction is difficult to measure precisely, but the significant decrease in output power can intuitively demonstrate the impact of an OC fault on the system's transmission performance, thereby highlighting the necessity of diagnosis. Simultaneously, such abrupt characteristics in transmission performance can also serve as supplementary verification for diagnostic results. In summary, the impact of a single-tube OC fault on transmission characteristics manifests as follows:

$$\begin{cases} P'_{out} = \dfrac{1}{4}P_{out} \\ \eta' < \eta \end{cases} \tag{18}$$

Fault diagnosis method based on DC bus voltage and switch driving signal

WPT system diagnostic model

The equivalent circuit of the WPT system used to establish the diagnostic model is shown in Fig. 4. The two arms of the inverter circuit are defined as the leading-leg and lagging-leg, respectively, and the switching function can be expressed as:

$$S_x = \begin{cases} 1, (S_{upper}, S_{lower}) = (1,0) \\ 0, (S_{upper}, S_{lower}) = (0,1) \end{cases} \quad x = \text{leading-leg, lagging-leg} \tag{19}$$

where, S_{upper} (S_{lower}) for the upper (lower) switching tube of the bridge arm.

The input current i_{dc} of the inverter circuit is composed of the current flowing through the leading-leg or lagging-leg:

$$i_{dc} = \sum_x S_x i_x \tag{20}$$

When S_x remains constant, the system is considered to be in a steady state, and the voltage U_{C5} across C_5 is equal to U_o. When S_x changes, the system is considered to be in a transient state, and $U_o = U_{L1} + U_{C5} - U_{LS}$, so the voltages across L_1 and L_S satisfy the following relationship:

$$U_{L1} = U_{LS} \tag{21}$$

Since the equivalent input impedance of the system remains unchanged, i_x remains constant when the system is in the steady state, while i_{dc} undergoes instantaneous changes when the system becomes transient[16]:

$$\frac{di_{dc}}{dt} = \Delta S_x \frac{di_s}{dt} \tag{22}$$

where, i_s is the current during the turn-on or turn-off process of the switching transistor.

According to Kirchhoff's current law, the change in i_{dc} is composed of the change in current i_{L1} in L_1 and the change in current i_{C5}

in C_5, while the changes in i_{L1} and i_{C5} generate induced voltages at the two ends of L_1 and L_S, respectively:

$$\begin{cases} \frac{di_{dc}}{dt} = \frac{di_{L1}}{dt} + \frac{di_{C5}}{dt} \\ U_{L1} = L_1 \frac{di_{L1}}{dt} \\ U_{LS} = L_S \frac{di_{C5}}{dt} \end{cases} \tag{23}$$

Since L_S is much smaller than L_1, it can be ignored. According to Eqs. (21) and (23), we obtain:

$$U_{LS} = L_S \frac{L_1}{L_1 + L_S} \cdot \frac{di_{dc}}{dt} \approx L_S \frac{di_{dc}}{dt} \tag{24}$$

The DC bus voltage U_{dc} consists of two mutually opposite voltages, U_{C5} and U_{LS}:

$$U_{dc} = U_{C5} - L_S \frac{di_{dc}}{dt} \tag{25}$$

As can be seen from Eq. (25), when the system is in a steady state, U_{dc} remains relatively constant. When entering a transient state, U_{dc} will accompany the corresponding pulse. Since the system operates in an underdamped mode, the pulse exhibits an oscillatory decay waveform characteristic, which can serve as a basis for fault diagnosis.

DC bus voltage characteristics based on switch drive signals

In system operating mode, the time required for parasitic capacitance charging and discharging is negligible compared to other modes. When analyzing the switching transistor turn-on and turn-off processes, both the leading-leg and the lagging-leg can exhibit the six operating conditions distinguished by the positive and negative values of i_x on the left side of Fig. 5. This paper only discusses the three typical cases where $i_x > 0$.

$S_x = 1$ condition: For a single bridge arm, i_x is conducted through the upper tube S_{upper} on that bridge arm.

$S_x = 0$ condition: Since the IGBT cannot conduct in reverse, i_x conducts through diode D_{lower}.

$S_x = 1$ to 0 condition: When S_x jumps from 1 to 0, S_{upper} gradually shuts down, accompanied by the gradual conduction of the anti-parallel diode D_{lower} on the lower tube of the bridge arm. At this point, the following relationship is satisfied:

$$\begin{cases} i_x = i_{xa} + i_{xb} \\ \frac{di_{dc}}{dt} = \frac{di_{xa}}{dt} < 0 \end{cases} \tag{26}$$

where, i_{xa} and i_{xb} represent the currents flowing through S_{upper} and D_{lower} during the turn-off process, respectively.

Substituting Eq. (26) into Eq. (25) yields the following: When S_x undergoes a transition, U_{dc} generates a corresponding positive pulse, followed by an oscillatory decay characteristic. When an OC fault occurs in the switch, if S_{upper} is open-circuited, under the condition of $i_x > 0$, regardless of how S_x changes, i_x can only flow through D_{lower}, as shown in Fig. 5d. At this point, $di_{dc}/dt = 0$, and the aforementioned pulse characteristics of U_{dc} disappear. However, under the condition of $i_x < 0$, current can still flow through D_{upper} or S_{lower}, unaffected by the fault, so U_{dc} retains its corresponding pulse characteristics. Similarly, if S_{lower} is open-circuited, under the condition of $i_x < 0$, i_x can only be conducted through D_{upper}, and the pulse characteristics of U_{dc} will also disappear. Therefore, by combining the disappearance of the DC bus voltage characteristics with the switch drive signals, precise diagnosis and localization of switch transistor OC faults can be achieved.

Fault diagnosis and localization strategy for the WPT system

Based on the above analysis, the WPT system power switch OC fault diagnosis and localization strategy flowchart proposed in this paper is shown in Fig. 6, as follows:

Step 1: Signal acquisition. First, define the switch function change quantity, which satisfies the following relationship:

$$\Delta S_x = S_x(t_k) - S_x(t_{k-1}) \text{ where, } \Delta S_x \in \{-1, 0, 1\} \tag{27}$$

where, t_{k-1} denotes the last sampling point before time t_k.

Since U_{dc} does not have a characteristic waveform when $\Delta S_x = 0$, but exhibits the aforementioned pulse oscillation characteristics when $\Delta S_x = \pm 1$, it is only necessary to collect the DC bus voltage signal $U_{dc}(t_f)$ corresponding to the moment when $\Delta S_x = \pm 1$.

Step 2: Fault diagnosis. If the collected $U_{dc}(t_f)$ exhibits the aforementioned voltage characteristics, it is determined that the system's

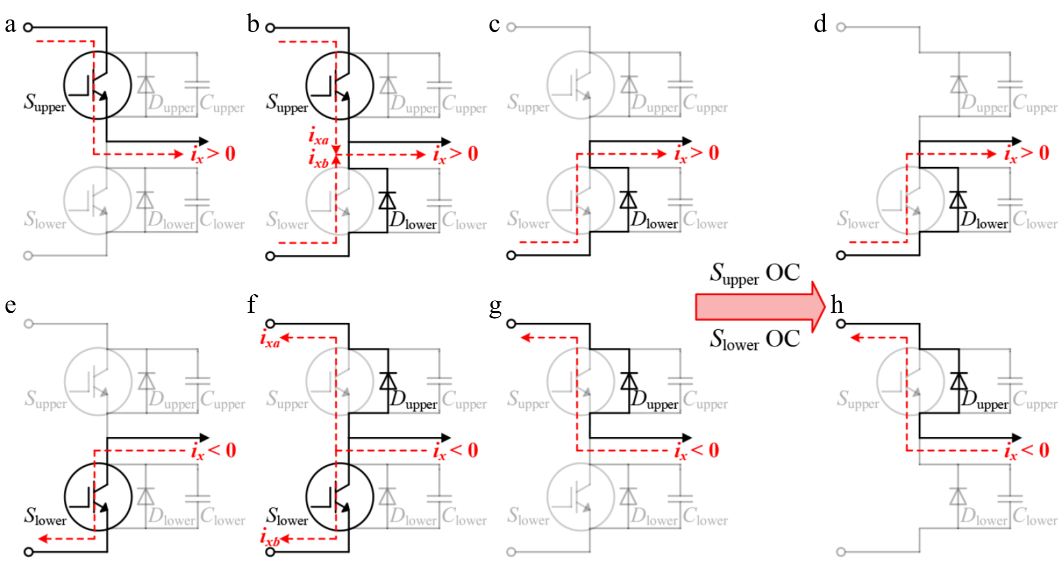

Fig. 5 Main current paths of the WPT system diagnostic model under different operating conditions. $i_x > 0$: (a) $S_x = 1$; (b) $S_x = 1$ to 0; (c) $S_x = 0$; (d) S_{upper} OC. $i_x < 0$: (e) $S_x = 0$; (f) $S_x = 0$ to 1; (g) $S_x = 1$; (h) S_{lower} OC.

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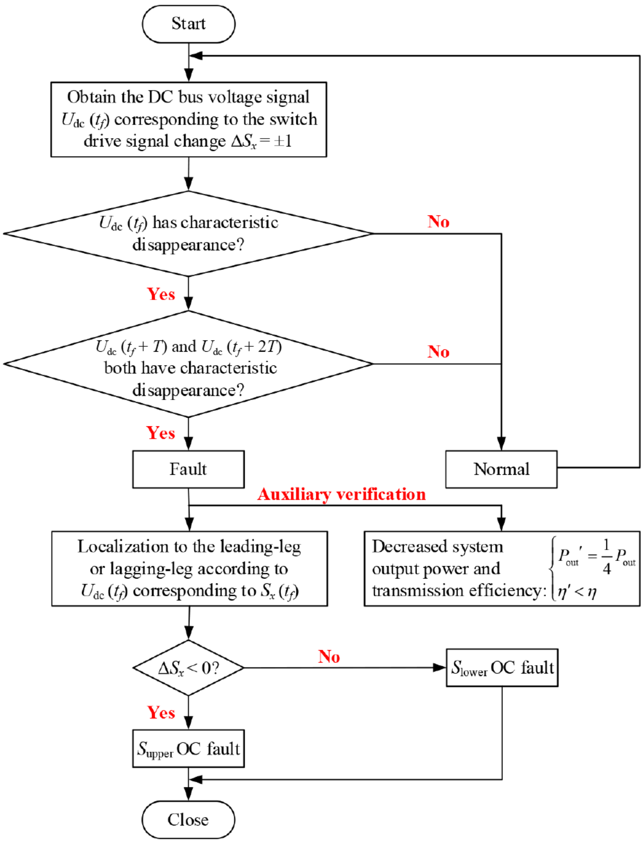

Fig. 6 Flowchart of WPT system fault diagnosis and localization strategy.

inverter circuit is functioning normally, and under normal operating conditions, U_{dc} typically exhibits four such characteristics within one cycle T. If the voltage characteristics of U_{dc} (t_f) disappear, it is determined that the system may have an OC fault in the power switch, and the fault verification process is initiated. If the characteristics of U_{dc} ($t_f + T$) and U_{dc} ($t_f + 2T$) disappear in the subsequent two cycles, the power switch OC fault is confirmed, and the process proceeds to the next step of fault localization. Otherwise, the system is still deemed to be operating normally. In actual experiments, the diagnostic threshold can be set reasonably to simplify the judgment logic. When the pulse amplitude of U_{dc} (t_f) is below this threshold, it is considered that the characteristic is missing.

Step 3: Fault location. Combining the timing information of U_{dc} (t_f), it is possible to first determine whether the fault occurred in the leading-leg or the lagging-leg. Further combining this with the positive or negative nature of ΔS_x, it is possible to locate the specific fault power switch. If $\Delta S_x > 0$, it is determined to be S_{lower} fault; if $\Delta S_x < 0$, it is determined to be S_{upper} fault.

Auxiliary verification step: Achieved by monitoring sudden characteristics in system transmission performance. If the system output power drops significantly to approximately one-quarter of the normal value while efficiency decreases slightly, this indicates an OC fault has occurred.

Analysis of experimental results

To validate the proposed method in this paper, an experimental platform as shown in Fig. 7 was constructed. Parameter measurements were performed using an Agilent E4980A LCR meter. The specific system parameter configuration is listed in Table 1, with parameter design satisfying the system input impedance constraints specified in Eq. (4). The inverter circuit employs the Infineon IKW75N65RH5 IGBT module, while the rectifier circuit utilizes the ThinkiSemi MUR40120PT fast recovery diode. In the experiment, the distance between the transmitting and receiving coils varied between 50 and 200 mm. The coupling coefficient k, calculated based on the measured mutual inductance, ranged from 0.384 to 0.098. According to the IGBT module datasheet, its equivalent output capacitance C_{oes} is approximately 460 pF. The t_d was set to 551 ns to satisfy the constraint requirement in Eq. (3).

The method of simulating an OC fault in the switching transistor via drive signal control from the host computer has been thoroughly validated[17]. This approach is also employed in the experiments described herein. Figure 8a–c, and d–f, respectively display the key electrical waveforms during normal system operation and S_2 OC fault conditions, with a coil spacing of 100 mm. The phase relationship between u_{in} and i_T in Fig. 8b and e confirm the system operates in ZVS mode. Following the fault, the negative half-cycle of u_{in} nearly vanishes. Combining Fig. 8b, c, e, and f reveals that both

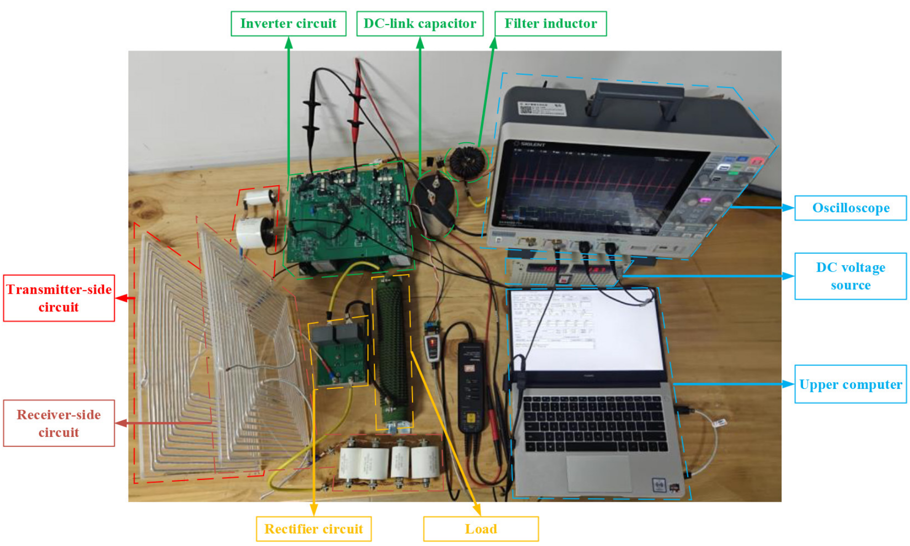

Fig. 7 Experimental platform for method validation.

Table 1. Experimental platform parameters.

Parameters	Value	Parameters	Value
U_o (V)	80	f (kHz)	70
δ (°)	19	t_d (ns)	551
L_1 (mH)	0.3	r_{L1} (Ω)	0.002
C_5 (mF)	0.5	r_{C5} (Ω)	0.013
L_S (nH)	218	r_{IGBT} (Ω)	0.06
t_r (ns)	9	t_f (ns)	15
C_{ce} (pF)	445	M (μH)	4.2~16.5
R_T (Ω)	0.06	R_R (Ω)	0.07
L_T (μH)	42.7	L_R (μH)	43.2
C_T (nF)	128.8	C_R (nF)	120.1
U_D (V)	1.7	r_D (Ω)	0.005
C_6 (μF)	50.2	r_{C6} (Ω)	0.005
R_L (Ω)	5.5~20.1	k	0.098~0.384

I_{Tm} and I_{Rm} decrease by approximately 50% post-fault. From the measured data in Fig. 8a–c, the normal operating conditions yield U_o = 80 V, I_o = 18 A, I_{Tm} = 26.3 A, I_{Rm} = 16 A, and U_{RL} = 114.9 V. Calculations based on these values indicate an output power of 1,269.424 W under normal conditions, with an actual operating efficiency of 88.2%. Substituting the normal operating electrical parameters into Eq. (14) yields a theoretical system efficiency of 90.6%, which closely matches the actual efficiency. Substituting the normal operating electrical parameters into Eq. (17) yields a theoretical efficiency of 88.3% after the system failure. As shown by the measured data in Fig. 8d and f, the actual efficiency after the failure is 84%, which is consistent with the theoretical analysis results, validating the conclusion of a slight decrease in efficiency post-failure. Simultaneous calculations show the pre- and post-fault output powers to be 1,269.424 and 309.124 W, respectively. The post-fault output power drops to approximately one-quarter of the pre-fault value, consistent with the theoretical analysis results presented earlier, thereby providing supplementary verification of the occurrence of an OC fault.

Figure 9 shows the DC bus voltage and drive signal waveforms for burst OC faults in each power switch under different coupling coefficients when the load resistance is fixed at 10.4 Ω. Taking the S_2 OC fault in Fig. 9a as an example: during normal operation, when the switching function S_x remains constant, U_{dc} stays relatively stable with minor noise; When S_x undergoes a sudden change, U_{dc} exhibits pronounced pulsed oscillation characteristics. After the fault occurs, the number of characteristic pulses generated within one cycle due to ΔS_x changes decreases from 4 to 3. By analyzing the timing relationship of the drive signal, it can be determined that the characteristic corresponding to $S_{leading\text{-}leg}$ arm has disappeared. Furthermore, since $\Delta S_x > 0$, the fault is further localized to the lower switch of this arm, i.e., S_2 is open-circuited. Based on the same diagnostic strategy, accurate diagnosis and localization are achieved for other OC faults of power switches shown in Fig. 9b–d, as well as for fault waveforms under different loads with a fixed coupling coefficient of 0.235, shown in Fig. 10, validating the effectiveness of the proposed method.

During the experiment, the U_{dc} signal was acquired using a high-voltage differential probe and simultaneously recorded by a SIGLENT SDS H12 Pro digital oscilloscope (sampling rate: 125 MSa/s). Additionally, to meet the requirements for long-term, high-speed data acquisition and online processing, a Yokogawa DL850E oscilloscope recorder (maximum sampling rate 100 MSa/s) was simultaneously employed for waveform recording. Based on this data, the diagnostic algorithm shown in Fig. 6 was executed, with results uploaded to the upper computer via a communication interface. In practical applications, since the required fault characteristics appear only during the instantaneous switching action, an intermittent sampling strategy can be adopted to effectively reduce the demand for continuous sampling rates in the system.

Discussion

Given the current lack of thorough research on fault diagnosis for WPT systems, this paper comprehensively compares several DC bus

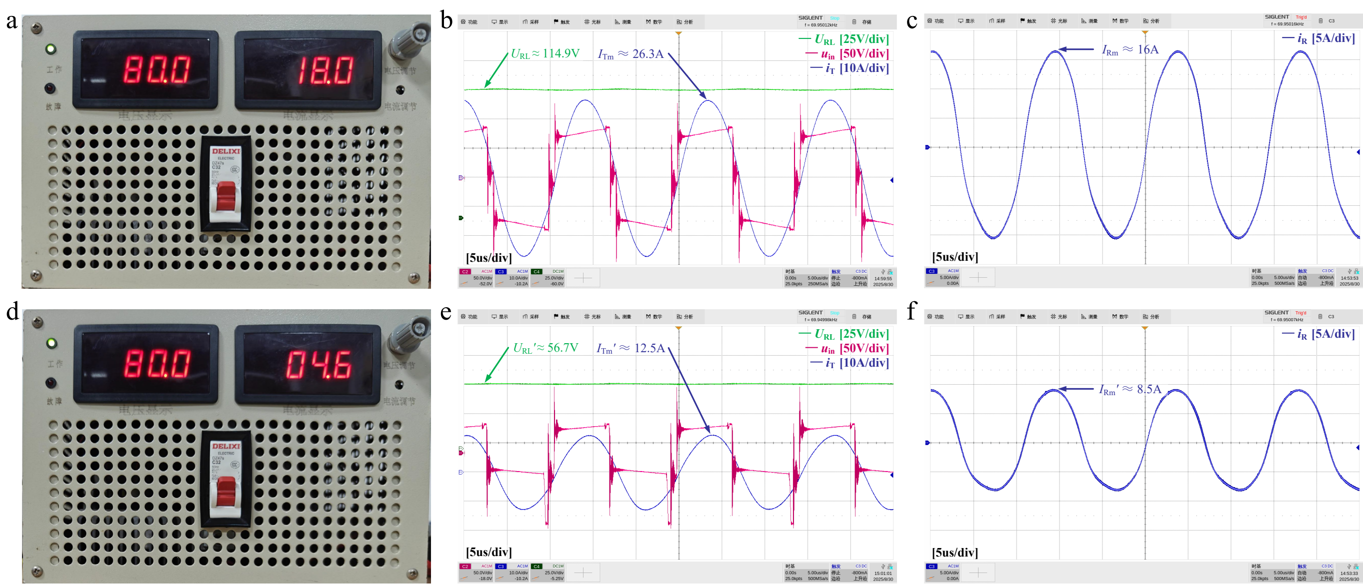

Fig. 8 Relevant electrical parameters for power and efficiency calculations. (a)–(c) Normal operating case. (d)–(f) S_2 OC case. (a) DC voltage source output voltage U_o and output current I_o. (b) Load voltage U_{RL}, inverter circuit output voltage u_{in}, and transmitter-side loop current i_T. (c) receiver-side loop current i_R. (d) DC voltage source output voltage U_o' and output current I_o'. (e) Load voltage U_{RL}', inverter circuit output voltage u_{in}', and transmitter-side loop current i_T'. (f) receiver-side loop current i_R'.

https://doi.org/10.48130/wpt-0026-0009

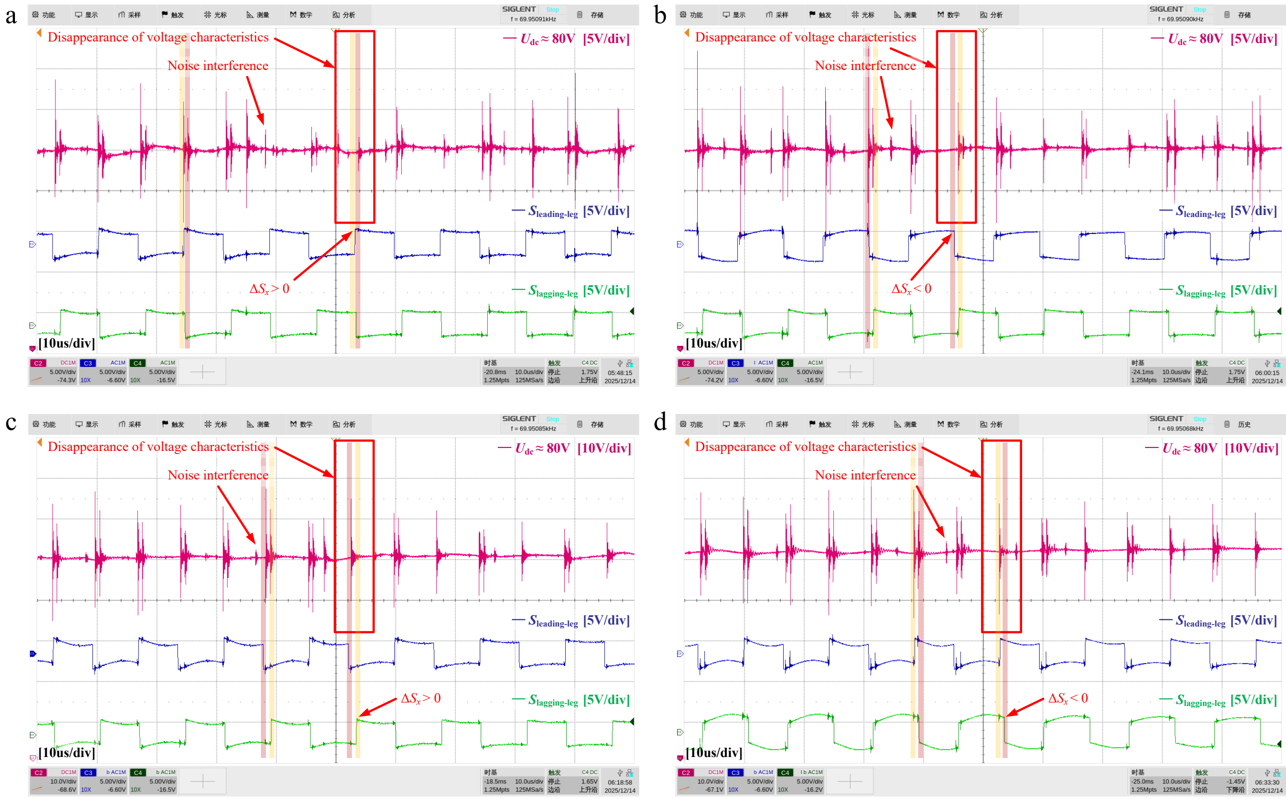

Fig. 9 Experimental results for OC fault in each switching transistor under different coupling coefficients. (a) $k = 0.384$, S_2 OC case. (b) $k = 0.235$, S_1 OC case. (c) $k = 0.158$, S_4 OC case. (d) $k = 0.098$, S_3 OC case.

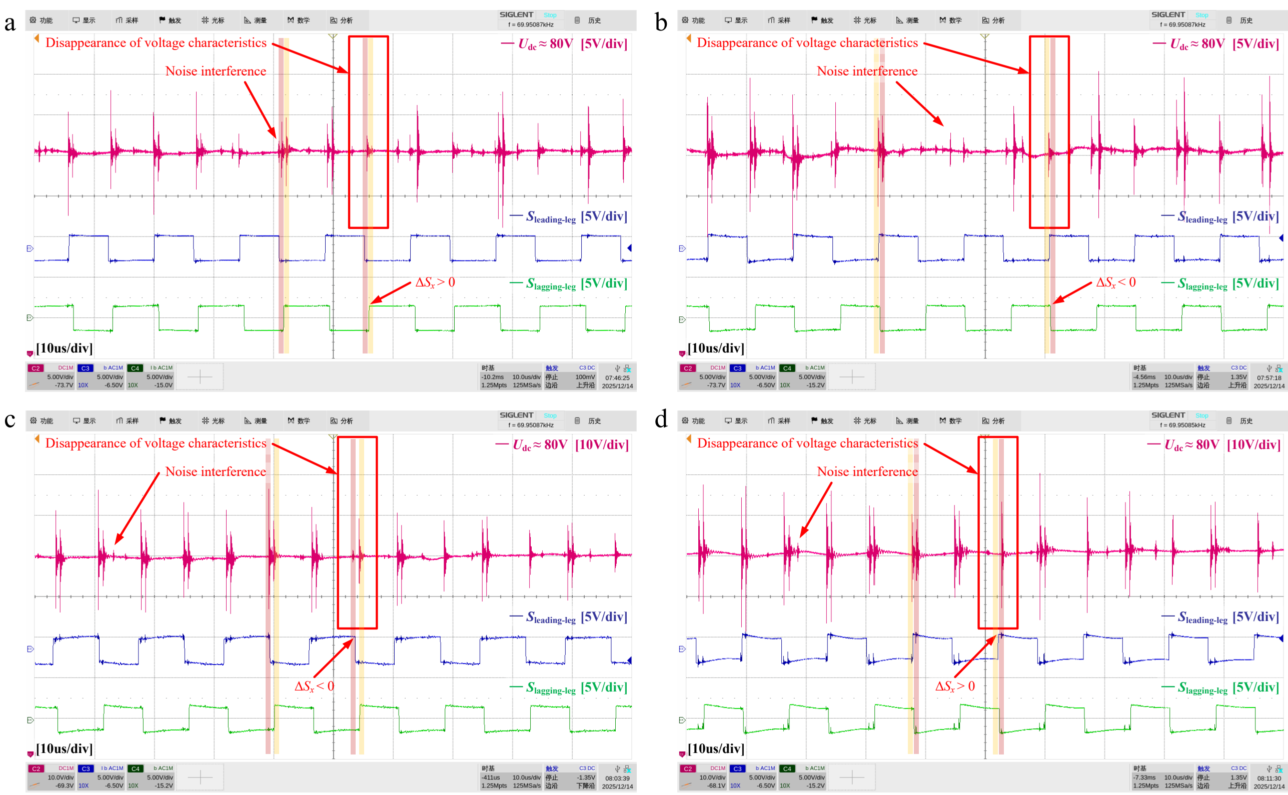

Fig. 10 Experimental results for OC fault in each switching transistor under different load resistances. (a) $R_L = 5.5\Omega$, S_4 OC case. (b) $R_L = 10.4\Omega$, S_3 OC case. (c) $R_L = 15.7\Omega$, S_1 OC case. (d) $R_L = 20.1\Omega$, S_2 OC case.

Table 2. Performance comparison of similar methods.

Ref.	Feature parameters	Diagnosis time	Software and hardware costs	Logical judgment
[18]	DC bus voltage difference residual	Three switching cycles	Medium	Comlex
[19]	DC capacitor voltage	One current cycle	Medium	Moderate
[20]	DC bus voltage, output current	Half to two current cycles	Small	Moderate
[21]	DC bus voltage, three-phase current	One switching cycle	Large	Moderate
Proposed	DC bus voltage	Three switching cycles	Small	Simple

voltage-based diagnostic methods in the power electronics field over recent years. The comparison is conducted across four dimensions—feature parameters, diagnostic time, cost, and judgment logic—to highlight the superiority of the proposed strategy. As shown in Table 2, the primary advantage of the proposed method lies in its straightforward diagnostic logic. To mitigate noise interference and ensure accuracy, it achieves precise fault localization within two to three switching cycles. Furthermore, as illustrated in Fig. 8, pulse oscillations are also observed on the inverter circuit output side when applying this method. This finding indicates that sufficient electrical margin must be reserved during switch device selection and driver circuit design. In subsequent work, the proposed method may struggle to precisely capture subtle electrical signal changes caused by device aging. Therefore, we will explore integrating machine learning methods to adaptively optimize diagnostic thresholds and achieve diagnosis of aging states resulting from device performance degradation.

Conclusions

This paper first analyzes the transmission characteristics of a WPT system when a single power switch experiences an OC fault. Subsequently, based on the current path when the system operates in ZVS mode, a fault diagnosis method for power switches is proposed using DC bus voltage and switch drive signals. This method achieves fault diagnosis and localization by identifying the disappearance of DC bus voltage characteristics. Experimental results confirm that the system's transmission characteristics post-fault align with theoretical analysis. When an OC fault occurs in the WPT system's power switch, the proposed method enables rapid and accurate fault localization within two to three switching cycles.

Author contributions

The authors confirm their contributions to the paper as follows: study conception and design: Chen C, Wang Z, Yu Y; data collection: Deng Q, Wang F; analysis and interpretation of results: Chen C, Wang F, Yu Y; draft manuscript preparation: Wang F, Wang Z. All authors reviewed the results and approved the final version of the manuscript.

Data availability

The datasets generated during and/or analyzed during the current study are available from the corresponding author upon reasonable request.

Acknowledgments

This work was supported in part by the National Natural Science Foundation of China under (Grant No. 52377128).

Conflict of interest

The authors declare that they have no conflict of interest.

Dates

Received 2 September 2025; Revised 22 December 2025; Accepted 28 February 2026; Published online 2 July 2026

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